

Application Serial No. 10/712,921  
Reply to office action of May 17, 2005

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PATENT  
Docket: CU-3455

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application: Chang Yeol LEE et al.

Serial No: 10/712,921

Filed: November 13, 2003

For: METHOD FOR REDUCING POLY-DEPLETION IN DUAL GATE CMOS  
FABRICATION PROCESS

] GRP ART UNIT: 2813

] Ex.: Chen, Jack S. J.

]

**Certification under 37 C.F.R. §1.8(a)**

The USPTO Central Fax No. (571) 273-8300

Date of Fax Transmittal: September 15, 2005

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted to the United States Patent and Trademark Office to the fax number and on the date indicated above.

  
W. William Park, Reg. No. 55,523

**AMENDMENT UNDER 37 CFR 1.111**

**Mail Stop Amendment**

The Commissioner for Patents  
P.O. Box 1450  
Alexandria VA 22313-1450

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Sir:

In response to the office action dated May 17, 2005, setting a 3-month shortened statutory period for a reply ending on August 17, 2005, the applicant submits the following responsive amendment in the above-identified application. This amendment is considered to place the application in better condition for allowance.

Also enclosed is the Request for One-Month Extension of Time, thereby extending the end date of the current term to September 17, 2005, accompanied by the authorization to charge the fee of \$120.00 to Deposit Account No. 12-0400. No other fee is believed to be required, but, if this is not the case, please charge any additional

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fee or credit any overpayment to Deposit Account No. 12-0400.

**Amendments to the Title** begin on page 3 of this paper.

**Amendments to the Specification** begin on page 4 of this paper.

**Amendments to the Claims** are reflected in the listing of claims, which begins  
on page 5 of this paper.

**Remarks/Arguments** begin on page 10 of this paper.

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**Amendments To The Title of the Invention**

Please replace the title of the present application with the following title:

—METHOD FOR REDUCING POLY-DEPLETION DUE TO THICKNESS  
VARIATION IN A POLYSILICON LAYER IN DUAL GATE CMOS FABRICATION  
PROCESS—